PATENT

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April 27, 2001
Date

Ayesha S. Wilks

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Ronnie M. Harrison	Attorney Docket No.	: 500395.02
Serial No.	: 09/758,970	Group Art Unit	: 2819
Filed	: January 4, 2001	Examiner	: Not Yet Assigned
Title	: METHOD AND APPARATUS FOR GENERATING A SEQUENCE OF CLOCK SIGNALS		

INFORMATION DISCLOSURE STATEMENT

Commissioner of Patents
Washington, D.C. 20231

Sir:

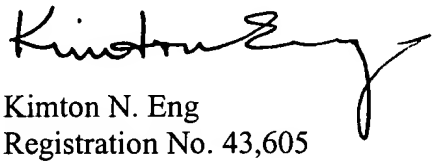
In accordance with 37 C.F.R. §§ 1.56 and 1.97 through 1.98, applicant wishes to make known to the Patent and Trademark Office the references set forth on the attached form PTO-1449. This application relies, under 35 U.S.C. § 120, on the earlier filing date of prior Application No. 08/879,847, filed June 20, 1997, issued January 9, 2001 as Patent No. 6,173,432. References AB-AE, AG-AH, AM, AO-AQ, AS-AT, AV, AX-AZ, BB-BK, BM, BQ-BV, BX-CB, CD, CF, CG, CJ, CK, CM-CP, CS, CT, CV-CZ, DA, DD-DH, DJ-DV, DX-DZ, EB, ED, EE, EK, EL, EN-ER, ET-EV, EX-FA, FC-FI, FM, FP, FS, FT, FV, FY, HN-HW, HY-IA, ID-IY, JA-JY, listed on the attached Form PTO-1449 were submitted to and/or cited by the Patent and Trademark Office in this prior application and, therefore, are not required to be provided in this application. If the Examiner wishes, copies will be provided upon request. Applicant also wishes to make known to the Patent and Trademark Office references AA, AF, AI-AL, AN, AR, AU, AW, BA, BL, BN-BP, BW, CC, CE, CH, CI, CL, CQ, CR, CU, CW-CY, DB-DC, DI, DW, EA, EC, EF-EJ, EM, ES, EW, FB, FJ-FL, FN, FO, FQ, FR, FU, FW, FX, FZ-HM, HX, IB, IC, IZ (copies of these cited references, as required under 37 C.F.R § 1.98, are enclosed). Although the aforesaid references are

made known to the Patent and Trademark Office in compliance with applicant's duty to disclose all information he is aware of which is believed relevant to the examination of the above-identified application, applicant believes that his invention is patentable.

Please acknowledge receipt of this Information Disclosure Statement and kindly make the cited references of record in the above-identified application.

Respectfully submitted,

DORSEY & WHITNEY LLP



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Enclosures:
Postcard
Form PTO-1449
Cited References (96)

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FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 500395.02	APPLICATION NO. 09/758,970
		APPLICANTS Ronnie M. Harrison	
		FILING DATE January 9, 2001	GROUP ART UNIT Not Yet Assigned

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	3,633,174	01/04/72	Griffin	340	172.5	
	AB	4,077,016	02/28/78	Sanders et al.	331	4	
	AC	4,096,402	06/20/78	Schroeder et al.	307	362	
	AD	4,404,474	09/13/83	Dingwall	307	260	
	AE	4,481,625	11/06/84	Roberts et al.	370	85	
	AF	4,508,983	04/02/85	Allgood et al.	307	577	
	AG	4,511,846	04/16/85	Nagy et al.	328	164	
	AH	4,514,647	04/30/85	Shoji	307	269	
	AI	4,524,448	06/18/85	Hullwegen	375	118	
	AJ	4,573,017	02/25/86	Levine	327	114	
	AK	4,600,895	07/15/86	Landsman	331	1 A	
	AL	4,603,320	07/29/86	Farago	341	89	
	AM	4,638,187	01/20/87	Boler et al.	307	451	
	AN	4,638,451	01/20/87	Hester et al.	395	889	
	AO	4,687,951	08/18/87	McElroy	307	269	
	AP	4,773,085	09/20/88	Cordell	375	120	
	AQ	4,789,796	12/06/88	Foss	307	443	
	AR	4,818,995	04/04/89	Takahashi et al.	341	94	
	AS	4,893,087	01/09/90	Davis	328	14	
	AT	4,902,986	02/20/90	Lesmeister	331	25	
	AU	4,953,128	08/28/90	Kawai et al.	365	194	
	AV	4,958,088	09/18/90	Farah-Bakhsh et al.	307	443	
	AW	4,972,470	11/20/90	Farago	380	3	
	AX	4,984,204	01/08/91	Sato et al.	365	189.11	
	AY	5,020,023	05/28/91	Smith	364	900	
	AZ	5,038,115	08/06/91	Myers et al.	331	2	

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INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		APPLICANTS Ronnie M. Harrison	
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U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	BA	5,075,569	12/24/91	Branson	307	270	
	BB	5,086,500	02/04/92	Greub	395	550	
	BC	5,087,828	02/11/92	Sato et al.	307	269	
	BD	5,122,690	06/16/92	Bianchi	307	475	
	BE	5,128,560	07/07/92	Chern et al.	307	475	
	BF	5,128,563	07/07/92	Hush et al.	307	482	
	BG	5,134,311	07/28/92	Biber et al.	307	270	
	BH	5,150,186	09/22/92	Pinney et al.	357	42	
	BI	5,165,046	11/17/92	Hesson	307	270	
	BJ	5,179,298	01/12/93	Hirano et al.	307	443	
	BK	5,194,765	03/16/93	Dunlop et al.	307	443	
	BL	5,212,601	05/18/93	Wilson	360	51	
	BM	5,220,208	06/15/93	Schenck	307	443	
	BN	5,223,755	06/29/93	Richley	307	603	
	BO	5,233,314	08/03/93	McDermott et al.	331	17	
	BP	5,233,564	08/03/93	Ohshima et al.	365	230.05	
	BQ	5,239,206	08/24/93	Yanai	307	272.2	
	BR	5,243,703	09/07/93	Farmwald et al.	395	325	
	BS	5,254,883	10/19/93	Horowitz et al.	307	443	
	BT	5,256,989	10/26/93	Parker et al.	331	1 A	
	BU	5,257,294	10/26/93	Pinto et al.	375	120	
	BV	5,268,639	12/07/93	Gasbarro et al.	324	158 R	
	BW	5,272,729	12/21/93	Bechade et al.	375	118	
	BX	5,274,276	12/28/93	Casper et al.	307	443	
	BY	5,276,642	01/04/94	Lee	365	189.04	
	BZ	5,278,460	01/11/94	Casper	307	296.5	

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U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	CA	5,281,865	01/25/94	Yamashita et al.	307	279	
	CB	5,283,631	02/01/94	Koerner et al.	307	451	
	CC	5,289,580	02/22/94	Latif et al.	395	275	
	CD	5,295,164	03/15/94	Yamamura	375	120	
	CE	5,304,952	04/19/94	Quiet et al.	331	1 A	
	CF	5,311,481	05/10/94	Casper et al.	365	230.06	
	CG	5,311,483	05/10/94	Takasugi	365	233	
	CH	5,313,431	05/17/94	Uruma et al.	365	230.05	
	CI	5,315,388	05/24/94	Shen et al.	348	718	
	CJ	5,321,368	06/14/94	Hoelzle	328	63	
	CK	5,337,285	08/09/94	Ware et al.	365	227	
	CL	5,341,405	08/23/94	Mallard, Jr.	375	120	
	CM	5,347,177	09/13/94	Lipp	307	443	
	CN	5,347,179	09/13/94	Casper et al.	307	451	
	CO	5,355,391	10/11/94	Horowitz et al.	375	36	
	CP	5,361,002	11/1/94	Casper	327	530	
	CQ	5,367,649	11/22/94	Cedar	395	375	
	CR	5,379,299	01/03/95	Schwartz	370	108	
	CS	5,390,308	02/14/95	Ware et al.	395	400	
	CT	5,400,283	03/21/95	Raad	365	203	
	CU	5,402,389	03/28/95	Flannagan et al.	365	233	
	CV	5,408,640	04/18/95	MacIntyre et al.	395	550	
	CW	5,410,263	04/25/95	Waizman	327	141	
	CX	5,416,436	05/16/95	Rainard	327	270	
	CY	5,416,909	05/16/95	Long et al.	395	275	
	CZ	5,420,544	05/30/95	Ishibashi	331	11	

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*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	DA	5,428,311	06/27/95	McClure	327	276	
	DB	5,428,317	06/27/95	Sanchez et al.	331	1 A	
	DC	5,430,408	07/04/95	Ovens et al.	327	407	
	DD	5,430,676	07/04/95	Ware et al.	365	189.02	
	DE	5,432,823	07/11/95	Gasbarro et al.	375	356	
	DF	5,438,545	08/01/95	Sim	365	189.05	
	DG	5,440,260	08/08/95	Hayashi et al.	327	278	
	DH	5,440,514	08/08/95	Flannagan et al.	365	194	
	DI	5,444,667	08/22/95	Obara	365	233	
	DJ	5,446,696	08/29/95	Ware et al.	365	222	
	DK	5,448,193	09/05/95	Baumert et al.	327	156	
	DL	5,451,898	09/19/95	Johnson	327	563	
	DM	5,457,407	10/10/95	Shu et al.	326	30	
	DN	5,465,076	11/07/95	Yamauchi et al.	331	179	
	DO	5,473,274	12/05/95	Reilly et al.	327	159	
	DP	5,473,575	12/05/95	Farmwald et al.	365	230.06	
	DQ	5,473,639	12/05/95	Lee et al.	375	376	
	DR	5,485,490	01/16/96	Leung et al.	375	371	
	DS	5,488,321	01/30/96	Johnson	327	66	
	DT	5,489,864	02/06/96	Ashuri	327	161	
	DU	5,497,127	03/05/96	Sauer	331	17	
	DV	5,498,990	03/12/96	Leung et al.	327	323	
	DW	5,500,808	03/19/96	Wang	364	578	
	DX	5,506,814	04/09/96	Hush et al.	365	230.03	
	DY	5,508,638	04/16/96	Cowles et al.	326	38	
	DZ	5,513,327	04/30/96	Farmwald et al.	395	309	

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*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	EA	5,532,714	07/02/96	Knapp et al.	345	114	
	EB	5,539,345	07/23/96	Hawkins	327	150	
	EC	5,544,124	08/06/96	Zagar et al.	365	230.08	
	ED	5,544,203	08/06/96	Casasanta et al.	375	376	
	EE	5,552,727	09/03/96	Nakao	327	159	
	EF	5,555,429	09/17/96	Parkinson et al.	395	800	
	EG	5,557,224	09/17/96	Wright et al.	327	115	
	EH	5,557,781	09/17/96	Stones et al.	395	550	
	EI	5,563,546	10/08/96	Tsukada	327	408	
	EJ	5,568,075	10/22/96	Curran et al.	327	172	
	EK	5,568,077	10/22/96	Sato et al.	327	199	
	EL	5,572,557	11/05/96	Aoki	375	376	
	EM	5,572,722	11/05/96	Vogley	395	555	
	EN	5,574,698	11/12/96	Raad	365	230.06	
	EO	5,576,645	11/19/96	Farwell	327	94	
	EP	5,577,236	11/19/96	Johnson et al.	395	551	
	EQ	5,578,940	11/26/96	Dillon et al.	326	30	
	ER	5,578,941	11/26/96	Sher et al.	326	34	
	ES	5,579,326	11/26/96	McClure	371	61	
	ET	5,581,197	12/03/96	Motley et al.	326	30	
	EU	5,589,788	12/31/96	Goto	327	276	
	EV	5,590,073	12/31/96	Arakawa et al.	365	185.08	
	EW	5,594,690	01/14/97	Rothenberger et al.	365	189.01	
	EX	5,614,855	03/25/97	Lee et al.	327	158	
	EY	5,619,473	04/08/97	Hotta	365	238.5	
	EZ	5,621,340	04/15/97	Lee et al.	327	65	

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EXAMINER INITIAL*		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	FA	5,621,690	04/15/97	Jungroth et al.	365	200	
	FB	5,621,739	04/15/97	Sine et al.	371	22.1	
	FC	5,627,780	05/06/97	Malhi	365	185.09	
	FD	5,627,791	05/06/97	Wright et al.	365	222	
	FE	5,631,872	05/20/97	Naritake et al.	365	227	
	FF	5,636,163	06/03/97	Furutani et al.	365	233	
	FG	5,636,173	06/03/97	Schaefer	365	230.03	
	FH	5,636,174	06/03/97	Rao	365	230.03	
	FI	5,638,335	06/10/97	Akiyama et al.	365	230.03	
	FJ	5,646,904	07/08/97	Ohno et al.	365	233	
	FK	5,652,530	07/29/97	Ashuri	326	93	
	FL	5,657,289	08/12/97	Hush et al.	365	230.05	
	FM	5,657,481	08/12/97	Farmwald et al.	395	551	
	FN	5,663,921	09/02/97	Pascucci et al.	365	233	
	FO	5,666,322	09/09/97	Conkle	365	233	
	FP	5,668,763	09/16/97	Fujioka et al.	365	200	
	FQ	5,668,774	09/16/97	Furatani	365	233	
	FR	5,675,274	10/07/97	Kobayashi et al.	327	158	
	FS	5,692,165	11/25/97	Jeddeloh et al.	395	551	
	FT	5,694,065	12/02/97	Hamasaki et al.	327	108	
	FU	5,708,611	01/13/98	Iwamoto	365	233 X	
	FV	5,712,580	01/27/98	Baumgartner et al.	327	12	
	FW	5,719,508	02/17/98	Daly	327	12	
	FX	5,740,123	04/14/98	Uchida	365	233	
	FY	5,751,665	05/12/98	Tanoi	368	120	
	FZ	5,767,715	06/16/98	Marquis et al.	327	159	

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	GA	5,768,177	06/16/98	Sakuragi	365	194	
	GB	5,778,214	07/07/98	Taya et al.	395	551	
	GC	5,781,499	07/14/98	Koshikawa	365	233	
	GD	5,784,422	07/21/98	Heermann	375	355	
	GE	5,789,947	08/04/98	Sato	327	3	
	GF	5,790,612	08/04/98	Chengson et al.	375	373	
	GG	5,794,020	08/11/98	Tanaka et al.	395	552	
	GH	5,805,931	09/08/98	Morzano et al.	395	884	
	GI	5,812,619	09/22/98	Runaldue	375	376	
	GJ	5,822,314	10/13/98	Chater-Lea	370	337	
	GK	5,831,929	11/03/98	Manning	365	233	
	GL	5,841,707	11/24/98	Cline et al.	365	194	
	GM	5,852,378	12/22/98	Keeth	327	171	
	GN	5,872,959	02/16/99	Nguyen et al.	395	552	
	GO	5,889,829	03/30/99	Chiao et al.	375	376	
	GP	5,898,674	04/27/99	Mawhinney et al.	370	247	
	GQ	5,917,760	06/29/99	Millar	365	194	
	GR	5,920,518	07/06/99	Harrison et al.	365	233	
	GS	5,926,047	07/20/99	Harrison	327	159	
	GT	5,926,436	07/20/99	Toda et al.	365	236	
	GU	5,940,608	08/17/99	Manning	395	551	
	GV	5,940,609	08/17/99	Harrison	395	559	
	GW	5,946,244	08/31/99	Manning	365	194	
	GX	5,953,284	09/14/99	Baker et al.	365	233	
	GY	5,964,884	10/12/99	Partovi et al.	713	503	
	GZ	5,990,719	11/23/99	Dai et al.	327	244	

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	HA	6,005,823	12/21/99	Martin et al.	365	230.08	
	HB	6,011,732	01/04/00	Harrison et al.	365	194	
	HC	6,016,282	01/18/00	Keeth	365	233	
	HD	6,026,050	02/15/00	Baker et al.	635	233	
	HE	6,029,250	02/22/00	Keeth	713	400	
	HF	6,038,219	03/14/00	Mawhinney et al.	370	242	
	HG	6,067,592	05/23/00	Farmwald et al.	710	104	
	HH	6,101,152	08/08/00	Farmwald et al.	365		
	HI	6,101,197	08/08/00	Keeth et al.	370	517	
	HJ	6,105,157	08/15/00	Miller	714	744	
	HK	6,160,423	12/12/00	Haq	327	41	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	HL	0 171 720 A2	02/19/86	EP			X	
	HM	6-1237512	10/22/86	JP (Abstract Only)			X	
	HN	0 295 515 A1	12/21/88	EP			X	
	HO	2-112317	4/25/90	JP (+ Abstract)				X
	HP	0 406 786 A1	1/9/91	EP			X	
	HQ	0 450 871 A2	10/9/91	EP			X	
	HR	0 476 585 A3	3/25/92	EP			X	
	HS	4-135311	5/8/92	JP (+ Abstract)				X
	HT	5-136664	6/1/93	JP (+ Abstract)				X
	HU	5-282868	10/29/93	JP (Abstract Only)			X	
	HV	WO 94/29871	12/22/94	PCT			X	

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FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 500395.02	APPLICATION NO. 09/758,970
		APPLICANTS Ronnie M. Harrison	
INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		FILING DATE January 9, 2001	GROUP ART UNIT Not Yet Assigned

	HW	0 655 741 A2	5/31/95	EP			X	
	HX	0 655 834 A1	5/31/95	EP			X	
	HY	WO 95/22200	8/17/95	PCT			X	
	HZ	WO 95/22206	8/17/95	PCT			X	
	IA	0 680 049 A2	11/2/95	EP			X	
	IB	0-7319577	12/8/95	JP (Abstract Only)			X	
	IC	0 703 663 A1	3/27/96	EP			X	
	ID	0 704 848 A3	4/3/96	EP			X	
	IE	0 704 975 A1	4/3/96	EP			X	
	IF	WO 96/10866	4/11/96	PCT			X	
	IG	0 767 538 A1	4/9/97	EP			X	
	IH	WO 97/14289	4/24/97	PCT			X	
	II	WO 97/42557	11/13/97	PCT			X	

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	IJ		Alvarez, J. et al. "A Wide-Bandwidth Low Voltage PLL for PowerPC ™ Microprocessors" IEEE IEICE Trans. Electron., Vol. E-78. No. 6, June 1995, pp. 631-639
	IK		Anonymous, "400MHz SLDRAM, 4M X 16 SLDRAM Pipelined, Eight Bank, 2.5 V Operation," SLDRAM Consortium Advance Sheet, published throughout the United States, pp.1-22
	IL		Anonymous, "Draft Standard for a High-Speed Memory Interface (SyncLink)", Microprocessor and Microcomputer Standards Subcommittee of the IEEE Computer Society, Copyright 1996 by the Institute of Electrical and Electronics Engineers, Inc., New York, NY, pp. 1-56
	IM		Anonymous, "Programmable Pulse Generator", IBM Technical Disclosure Bulletin, Vol. 17, No. 12, May 1975, pp. 3553-3554
	IN		Anonymous, "Pulse Combining Network", IBM Technical Disclosure Bulletin, Vol. 32, No. 12, May 1990, pp. 149-151
	IO		Anonymous, "Variable Delay Digital Circuit", IBM Technical Disclosure Bulletin, Vol. 35, No. 4A, September 1992, pp. 365-366

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	IP		Arai, Y. et al., "A CMOS Four Channel x 1K Time Memory LSI with 1-ns/b Resolution", IEEE Journal of Solid-State Circuits, Vol. 27, No. 3, M, 8107 March, 1992, No. 3, New York, US, pp. 359-364 and pp. 528-531
	IQ		Arai, Y. et al., "A Time Digitizer CMOS Gate-Array with a 250 ps Time Resolution", XP 000597207, IEEE Journal of Solid-State Circuits, Vol. 31, No.2, February 1996, pp. 212-220
	IR		Aviram, A. et al., "OBTAINING HIGH SPEED PRINTING ON THERMAL SENSITIVE SPECIAL PAPER WITH A RESISTIVE RIBBON PRINT HEAD", IBM Technical Disclosure Bulletin, Vol. 27, No. 5, October 1984, pp. 3059-3060
	IS		Bazes, M., "Two Novel Fully Complementary Self-Biased CMOS Differential Amplifiers", IEEE Journal of Solid-State Circuits, Vol. 26, No. 2, February 1991, pp. 165-168
	IT		Chapman, J. et al., "A Low-Cost High-Performance CMOS Timing Vernier for ATE", IEEE International Test Conference, Paper 21.2, 1995, pp. 459-468
	IU		Cho, J. "Digitally-Controlled PLL with Pulse Width Detection Mechanism for Error Correction", ISSCC 1997, Paper No. SA 20.3, pp. 334-335
	IV		Christiansen, J., "An Integrated High Resolution CMOS Timing Generator Based on an Array of Delay Locked Loops", IEEE Journal of Solid-State Circuits, Vol. 31, No. 7, July 1996, pp. 952-957
	IW		Combes, M. et al., "A Portable Clock Multiplier Generator Using Digital CMOS Standard Cells", IEEE Journal of Solid-State Circuits, Vol. 31, No. 7, July 1996, pp. 958-965
	IX		Donnelly, K. et al., "A 660 MB/s Interface Megacell Portable Circuit in 0.3 μm-0.7 μm CMOS ASIC", IEEE Journal of Solid-State Circuits, Vol. 31, No. 12, December 1996, pp. 1995-2001
	IY		Goto, J. et al., "A PLL-Based Programmable Clock Generator with 50- to 350-MHz Oscillating Range for Video Signal Processors", IEICE Trans. Electron., Vol. E77-C, No. 12, December 1994, pp. 1951-1956
	IZ		Gustavsion, David B., et al., "IEEE Standard for Scalable Coherent Interface (SCI)," IEEE Computer Society, IEEE Std. 1596-1992, August 2, 1993.
	JA		Hamamoto, T., "400-MHz Random Column Operating SDRAM Techniques with Self-Skew Compensation", IEEE Journal of Solid-State Circuits, Vol. 33, No. 5, May 1998, pp. 770-778
	JB		Ishibashi, A. et al., "High-Speed Clock Distribution Architecture Employing PLL for 0.6μm CMOS SOG", IEEE Custom Integrated Circuits Conference, 1992, pp. 27.6.1-27.6.4
	JC		Kim, B. et al., "A 30MHz High-Speed Analog/Digital PLL in 2μm CMOS", ISSCC, February 1990

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	JD		Kikuchi, S. et al., "A GATE-ARRAY-BASED 666MHz VLSI TEST SYSTEM", IEEE International Test Conference, Paper 21.1, 1995, pp. 451-458
	JE		Ko, U. et al., "A 30-ps JITTER, 3.6-μs LOCKING, 3.3-VOLT DIGITAL PLL FOR CMOS GATE ARRAYS", IEEE Custom Integrated Circuits Conference, 1993, pp. 23.3.1-23.3.4
	JF		Lee, T. et al., "A 2.5V Delay-Locked Loop for an 18Mb 500MB/s DRAM", IEEE International Solid-State Circuits Conference Digest of Technical Papers, Paper No. FA 18.6, 1994, pp. 300-301
	JG		Lesmeister, G., "A DENSELY INTEGRATED HIGH PERFORMANCE CMOS TESTER", International Test Conference, Paper 16.2, 1991, pp. 426-429
	JH		Ljuslin, C. et al., "An Integrated 16-channel CMOS Time to Digital Converter", IEEE Nuclear Science Symposium & Medical Imaging Conference Record, Vol. 1, 1993, pp. 625-629
	JI		Maneatis, J., "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1723-1732
	JJ		Nakamura, M. et al., "A 156 Mbps CMOS Clock Recovery Circuit for Burst-mode Transmission", Symposium on VLSI Circuits Digest of Technical Papers, 1996, pp. 122-123
	JK		Nielson, E., "Inverting latches make simple VCO", EDN, June 19, 1997
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	JM		Saeki, T. et al., "A 2.5-ns Clock Access, 250-MHz, 256-Mb SDRAM with Synchronous Mirror Delay", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1656-1665
	JN		Santos, D. et al., "A CMOS Delay Locked Loop And Sub-Nanosecond Time-to-Digital Converter Chip", IEEE Nuclear Science Symposium and Medical Imaging Conference Record, Vol. 1, October 1995, pp. 289-291
	JO		Shirotori, T. et al., "PLL-based, Impedance Controlled Output Buffer", 1991 Symposium on VLSI Circuits Digest of Technical Papers, pp. 49-50.
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	JQ		Sidiropoulos, S. et al., "A CMOS 500 Mbps/pin synchronous point to point link interface", IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1994, pp. 43-44

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	JR		Sidiropoulos, S. et al., "A Semi-Digital DLL with Unlimited Phase Shift Capability and 0.08-400MHz Operating Range," IEEE International Solid State Circuits Conference, February 8, 1997, pp.332-333
	JS		Soyuer, M. et al., " A Fully Monolithic 1.25GHz CMOS Frequency Synthesizer", IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1994, pp. 127-128
	JT		Taguchi, M. et al., "A 40-ns 64-Mb DRAM with 64-b Parallel Data Bus Architecture", IEEE Journal of Solid-State Circuits, Vol. 26, No. 11, November 1991, pp. 1493-1497
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	JV		Tanoi, S. et. al., "A 250-622 MHz Deskew and Jitter-Suppressed Clock Buffer Using Two-Loop Architecture", IEEE IEICE Trans. Electron., Vol.E-79-C. No. 7, July 1996, pp.898-904
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	JX		Watson, R. et al., "Clock Buffer Chip with Absolute Delay Regulation Over Process and Environmental Variations", IEEE Custom Integrated Circuits Conference, 1992, pp. 25.2.1-25.2.5
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	JZ		

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